

Attorney's Docket No. 2998P035  
Confirmation No.: 3004

*ITW*  
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Wolf-Dietrich Weber,

Application No.: 10/698,905

Filed: October 31, 2003

For: METHOD AND APPARATUS FOR  
ESTABLISHING A QUALITY OF  
SERVICE MODEL

Examiner: Unassigned

Art Unit: 2825

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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Dianne Neathery

(Typed or printed name of person mailing correspondence)

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Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

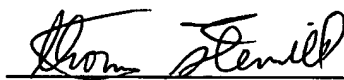
- X   37 C.F.R. §1.97(b).
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: August 22, 2005



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<b>Substitute for Form 1449/PTO</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>				<b>Complete if Known</b>	
				Application Number	10/698,905
				Filing Date	October 31, 2003
				First Named Inventor:	Wolf-Dietrich Weber
				Art Unit	2825
				Examiner Name	Not yet assigned
Sheet	2	of	3	Attorney Docket Number	2998P035
<b>NON PATENT LITERATURE DOCUMENTS</b>					
Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T <sup>2</sup>
	2	WOLF-DIETRICH WEBER, et al., " <i>A quality-of-service mechanism for interconnection networks inn system-on-chips</i> ", IEEE 2005, 6 pages.			
	3	DREW WINGARD, " <i>MicroNetworks-Based Integration for SOC's.</i> " In Design Automation Conference, 2001, pp. 673-677, 5 pages.			
	4	PAUL WIELAGE, et al., " <i>Networks on Silicon: Blessing or Nightmare?</i> " Keynote speech, Proceedings of the Euromicro Symposium on Digital System Design, Dortmund, Germany, September 2002, 5 pages.			
	5	RON HO, et al., " <i>The Future of Wires</i> ". In Proceedings of the IEEE, Vol. 89, No. 4, pp. 490-504, April 2001, 15 pages.			
	6	WILLIAM J. DALLY, et al., " <i>Route Packets, Not Wires: On-Chip Interconnection Networks.</i> " In Design Automation Conference, pp. 684-689, June 2001, 6 pages.			
	7	LUCA BENINI, et al., " <i>Networks on Chips: A New SoC Paradigm</i> ", In IEEE 2002, Computer, Vol. 35, No. 1, pp.70-78, 9 pages.			
	8	JIM KUROSE, " <i>Open Issues and Challenges in Providing Quality of Service Guarantees in High-Speed Networks</i> ", ACM Computer Communication Review, Vol. 23, No. 1, pp.6-15, January 1993, 10 pages.			
	9	MARTIN REISSLEIN et al., " <i>A Framework for Guaranteeing Statistical QoS</i> ", In IEEE/ACM Transactions on Networking, Vol. 10, No. 1, February 2002, pp.27-42, 16 pages.			
	10	HUI ZHANG, " <i>Service Disciplines for Guaranteed Performance Service in Packet-Switching Networks</i> ", Proceedings of the IEEE, Vol. 83, No. 10, October 1995, pp.1374-1396, 23 pages.			
	11	DIMITRIOS STILIADIS, et al., " <i>Latency-Rate Servers: A General Model for Analysis of Traffic Scheduling Algorithms</i> ", In Proceedings of IEEE INFOCOM 96, April 1996, pp.111-119, 9 pages.			

Examiner Signature		Date Considered	
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\*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	12	K. GOOSSENS, et al., " <i>Networks on Silicon: Combining Best-Effort and Guaranteed Services</i> ", In Proceeding of 2002 Design, 3 pages.			
	13	E. RIJPKEMA, et al., " <i>Trade Offs in the Design of a Router with Both Guaranteed and Best-Effort Services for Networks on Chip</i> ", In Proceedings of Design Automation and Test Conference in Europe, March 2003, 6 pages.			
	14	K. LAHIRI, et al., " <i>LOTTERYBUS: A New High-Performance Communication Architecture for System-on-Chip Designs</i> ". In Proceedings of Design Automation Conference 2003, Las Vegas, June 2001, pp.15-20, 6 pages.			
	15	WILLIAM J. DALLY, " <i>Virtual-channel Flow Control</i> ", In Proceedings of the 17th Int. Symp. on Computer Architecture, ACM SIGARCH, May 1990, Vol. 18, No. 2, pp. 60-68, 9 pages.			
	16	DREW WINGARD, et al., " <i>Integration Architecture for System-on-a-Chip Design</i> ", In Proc. of the 1998 Custom Integrated Circuits Conference, May 1998, pp 85-88, 4 pages.			
	17	AXEL JANTSCH, et al., " <i>Networks on Chip</i> ", Kluwer Academic Publishers, 2003. Cover, Title Page, Contents, (4 pp.) Chapters 1-5, (pp.3-106,) Chapters 7-8, (pp.131-172) & Chapter10, (pp. 193-213), 171 pages.			
	18	WEBER, WOLF-DIETRICH, et al., "Enabling Reuse via an IP Core-centric Communications Protocol: Open Core Protocol", In Proceedings of the IP 2000 System-on-Chip Conference March 2000, pp.1-5.			

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